What is claimed is:

1. A non-volatile memory comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks; and

read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from a second one of the plurality of addressable banks.

2. The non-volatile memory of claim 1 wherein the read/write circuitry comprises a write latch to store the first data provided on external data communication connections.

3. The non-volatile memory of claim 1 wherein the plurality of addressable banks comprise four blocks.

4. The non-volatile memory of claim 1 wherein the read/write circuitry receives the first data from a first external processor, and the read/write circuitry provides the second data in response to a second external processor.

5. The non-volatile memory of claim 1 wherein the read/write circuitry writes the first data to an array row of the first one of the plurality of addressable banks and simultaneously reads second data from the array row of the second one of the plurality of addressable banks.

6. The non-volatile memory of claim 1 wherein the non-volatile memory is a synchronous non-volatile memory.

7. A non-volatile memory comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks;

a write latch to store first data provided on external data communication connections; and

read/write circuitry coupled to the array, wherein the read/write circuitry writes the first data to a first one of the plurality of addressable banks and simultaneously reads second data from a second one of the plurality of addressable banks.

8. The non-volatile memory of claim 7 wherein the read/write circuitry receives the first data from a first external processor, and the read/write circuitry provides the second data in response to a second external processor.

9. A processing system comprising:

a processor; and

a non-volatile memory coupled to the processor and comprising,

an array of non-volatile memory cells arranged in a plurality of addressable banks, and

read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the processor to a first one of the plurality of addressable banks and simultaneously reads second data from a second one of the plurality of addressable banks and provides the second data to the processor.

10. The processing system of claim 9 further comprising a write latch to store the first data.

11. A processing system comprising:

first and second processors; and

a non-volatile memory coupled to the first and second processors, the non-volatile memory comprises,

an array of non-volatile memory cells arranged in a plurality of addressable banks,

a data latch coupled to the array to store write data, and

read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the first processor to a first one of the plurality of addressable banks and simultaneously reads second data from a second one of the plurality of addressable banks and provides the second data to the second processor.

12. A method of operating a non-volatile memory comprising:

writing first data to a first bank location in a memory array of the non-volatile memory; and

substantially simultaneously reading second data from a second bank location in the memory array of the non-volatile memory.

13. The method of claim 12 wherein the first data is provided to the non-volatile memory via an external processor.

14. The method of claim 12 wherein the first data is provided to the non-volatile memory via a first external processor, and the method further comprises outputting the second data to a second external processor.

15. The method of claim 12 further comprising accessing a common addressable row of the first and second blank locations prior to writing the first data and reading the second data.

16. The method of claim 12 wherein writing the first data comprises storing the first data in a latch circuit prior to writing the first data to the first bank location in the memory array.

17. A method of operating a memory device comprising:

receiving first externally provided data;

storing the first data in a write latch;

writing the first data from the write latch to a first bank location in a memory array of the memory; and

substantially simultaneously reading second data from a second bank location in the memory array of the memory.

18. The method of claim 17 wherein the first data is provided by an external processor.

19. The method of claim 18 further comprising outputting the second data to the external processor.

20. The method of claim 17 wherein the first data is provided by a first external processor, and the method further comprises outputting the second data to a second external processor.

21. A method of operating a non-volatile memory device comprising:

receiving first data from a first external processor coupled to the memory;

storing the first data in a write latch;

writing the first data from the write latch to a first location in a memory array of the non-volatile memory device;

substantially simultaneously reading second data from a second location in the memory array of the non-volatile memory device; and

outputting the second data to a second external processor coupled to the memory device.

22. The method of claim 21 wherein the first and second locations are first and second addressable blocks of the memory array.

23. The method of claim 22 wherein the first data is written to a row of the first block and the second data is read from a common row of the second block.